National Semiconductor

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ADC12QS065 Quad 12-Bit 65 MSPS A/D Converter with LVDS Serialized Outputs

General Description

The ADC12QS065 is a low power, high performance CMOS 4-channel analog-to-digital converter with LVDS serialized outputs. The ADC12QS065 digitizes signals to 12 bits resolution at sampling rates up to 65 MSPS while consuming a typical 200 mW/ADC from a single 3.3V supply. Sampled data is transformed into high speed serial LVDS output data streams. Clock and frame LVDS pairs aid in data capture. The ADC12QS065's six differential pairs transmit data over backplanes or cable and also make PCB design easier. In addition, the reduced cable, PCB trace count, and connector size tremendously reduce cost.

No missing codes performance is guaranteed over the full operating temperature range. The pipeline ADC architecture achieves 11 Effective Bits over the entire Nyquist band at 65 MSPS.

When not converting, power consumption can be reduced by pulling the PD (Power Down) pin high, placing the converter into a low power state where it typically consumes less than 3 mW total, and from which recovery is less than 5 ms. The ADC12QS065's speed, resolution and single supply operation makes it well suited for a variety of applications in ultrasound, imaging, video and communications. Operating over the industrial (-40°C to +85°C) temperature range, the ADC12QS065 is available in a 60 pin LLP package with exposed pad (9x9x0.8mm, 0.5mm pin pitch).

Features

- Single +3.3V supply operation
- Internal sample-and-hold and Internal reference
- Low power consumption
- Power down mode
- Clock and Data Frame Timing
- 780 Mbps serial LVDS data rate (at 65 MHz clock)
- LVDS serial output rated for 100 Ohm load

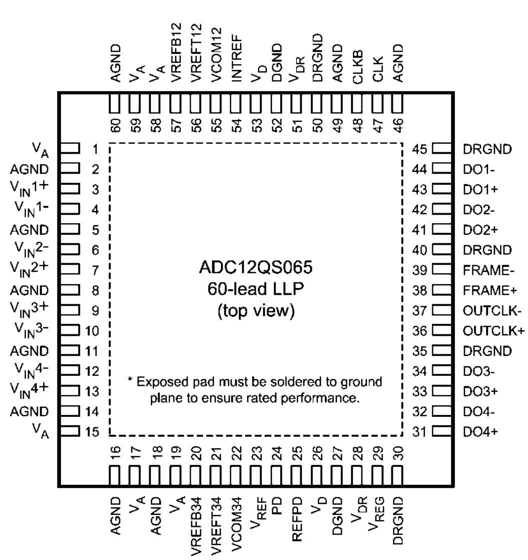
Key Specifications

Resolution	12 Bits
DNL	±0.3 LSB (typ)
SNR (f_{IN} = 5 MHz)	69 dB (typ)
SFDR (f_{IN} = 5 MHz)	83 dB (typ)
ENOB (at Nyquist)	11 Bits (typ)
Power Consumption	
-- Operating, 65 MSPS, per ADC	200 mW (typ)
-- Power Down Mode	< 3 mW (typ)

Applications

- Ultrasound
- Medical Imaging
- Communications
- Portable Instrumentation
- Digital Video

Connection Diagram



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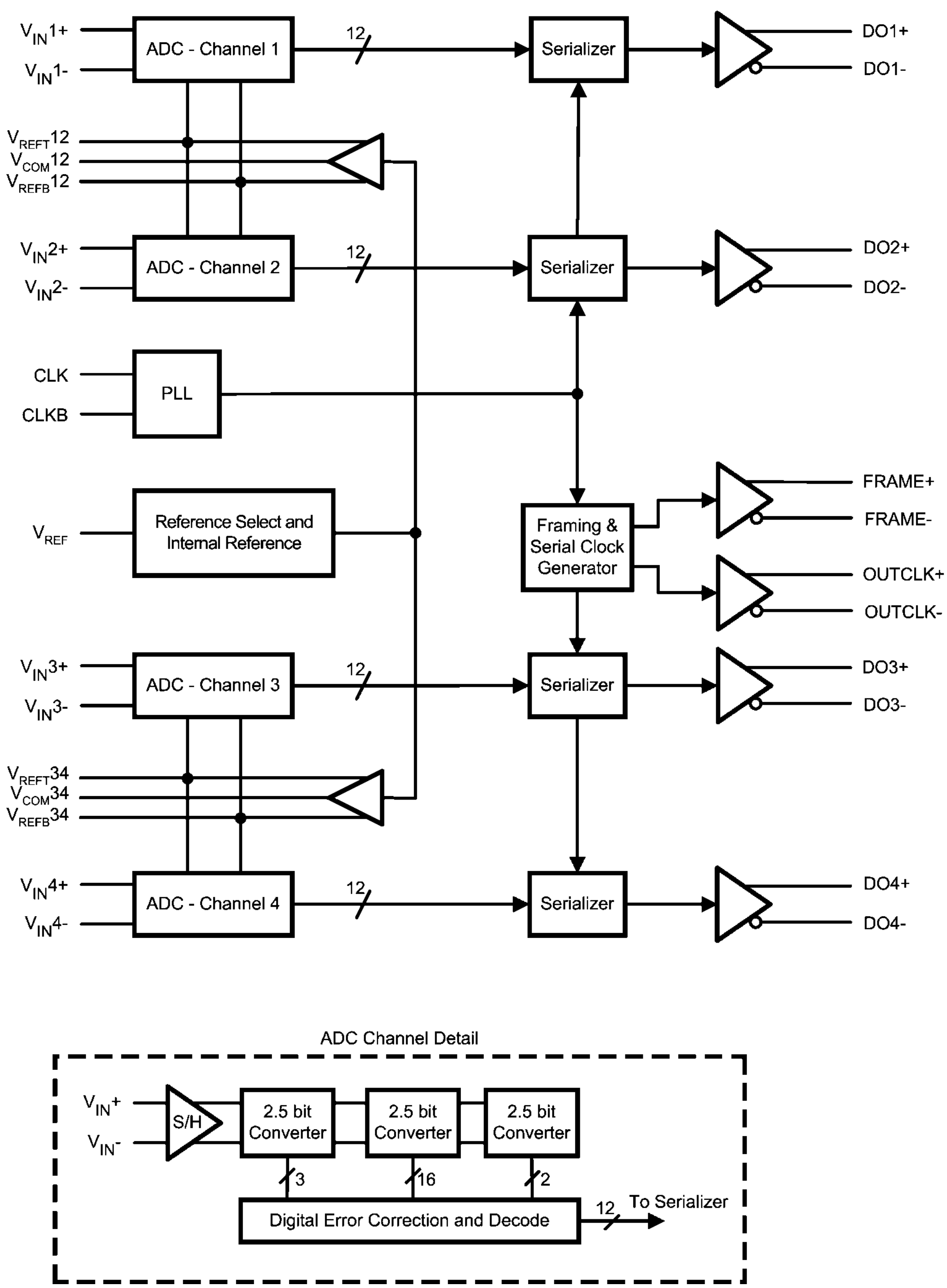
Ordering Information

Industrial (−40°C ≤ T_A ≤ +85°C)	Package
ADC12QS065CISQ	60 Pin LLP
ADC12QS065EVAL	Evaluation Board

Block Diagram



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Pin Descriptions

Pin No.	Symbol	Description
ANALOG I/O		
3 7 9 13	$V_{IN}1+$ $V_{IN}2+$ $V_{IN}3+$ $V_{IN}4+$	Differential analog input pins. With a 1.0V reference voltage the differential full-scale input signal level is 2.0 V_{P-P} with each input pin voltage centered on a common mode voltage, V_{COM}. The negative input pins may be connected to V_{COM} for single-ended operation, but a differential input signal is required for best performance.
4 6 10 12	$V_{IN}1-$ $V_{IN}2-$ $V_{IN}3-$ $V_{IN}4-$	
23	V_{REF}	This pin is the reference select pin and the external reference input, used in conjunction with the INTREF pin. If the INTREF pin is set to V_A , this pin is used as an internal reference select. With $V_{REF} = V_A$, the internal 1.0V reference is selected. With V_{REF}=AGND, the internal 0.5V reference is selected. If the INTREF pin is set to AGND, then this pin is the input for an external reference. A voltage in the range of 0.8 to 1V may be applied to this pin. V_{REF} should be bypassed to AGND with a 1.0 µF capacitor when an external reference is used.
56 21	VREFT12 VREFT34	Top ADC Reference. This pin has to be driven to 1.9V if REFPD is high. If REFPD is low, bypass this pin with a 0.1 µF low ESR capacitor to AGND and a 10 µF low ESR capacitor to VREFB. These pins should not be loaded.
55 22	VCOM12 VCOM34	This is an analog output which can be used as a common mode voltage for the inputs. It should be bypassed to AGND with a minimum of a 1.0 µF low ESR capacitor in parallel with a 0.1 µF capacitor. These pins may also be used as a 1.5V temperature stable reference voltage with a maximum load of 1mA.
57 20	VREFB12 VREFB34	Bottom ADC Reference. This pin has to be driven to 0.9V if REFPD is high. If REFPD is low, bypass this pin with a 0.1 µF low ESR capacitor to AGND and a 10 µF low ESR capacitor to VREFT. These pins should not be loaded.
29	VREG	This is the bypass pin for the internal 1.8V regulator. This pin should be bypassed to AGND with a 1.0 µF capacitor
DIGITAL I/O		
47	CLK	This pin acts as either a Non-Inverting Differential Clock input or a CMOS clock input. If CLKB is used as the Inverting Clock input, CLK will act as the Non-Inverting Clock input. If CLKB is tied to AGND, CLK will act as a CMOS clock input. ADC power consumption will increase by about 40mW if a Differential Clock is used.
48	CLKB	Inverting Differential Clock input. If tied to AGND, CLK acts as a CMOS clock input.
54	INTREF	Internal reference enable input. When this pin is high, two internal reference choices are selectable through the V_{REF} pin. When this pin is low, an external reference must be applied to V_{REF} (pin 23).
24	PD	Power Down pin that, when high, puts the converter into the Power Down mode.
25	REFPD	With REFPD high, user must drive VREFT12, VREFT34 and VREFB12 & VREFB34 externally. With REFPD low, VREFT12, VREFT34 and VREFB12 & VREFB34 are driven internally.
43 41 33 31	DO1+ DO2+ DO3+ DO4+	+ Serial Data Output. Non-inverting LVDS differential output.
44 42 34 32	DO1- DO2- DO3- DO4-	- Serial Data Output. Inverting LVDS differential output.
38 39	FRAME+ FRAME-	LVDS output, it's rising edge corresponds to the first serial bit of the output streams. FRAME clock frequency is the same as the CLK frequency.

Pin No.	Symbol	Description
36 37	OUTCLK+ OUTCLK-	LVDS output clock. The data is valid on an output transition. Successive data bits are captured on both edges of this clock. OUTCLK frequency is 6X the CLK frequency.
ANALOG POWER		
1,15,17,19, 58,59	V_A	Positive analog supply pins. These pins should be connected to a quiet +3.3V source and bypassed to AGND with 0.1 µF capacitors located near these power pins, and with a 10 µF capacitor.
2,5,8,11, 14,16,18, 46,49,60	AGND	The ground return for the analog supply. NOTE: The exposed pad on the LLP package must be soldered to AGND.
DIGITAL POWER		
26,53	V_D	Positive digital supply pin. This pin should be connected to the same quiet +3.3V source as is V_A and be bypassed to DGND with a 0.1 µF capacitor located near the power pin and with a 10 µF capacitor.
27,52	DGND	The ground return for the digital supply.
28, 51	V_{DR}	Positive driver supply pin for the ADC12QS065's output drivers. This pin should be connected to a voltage source of +2.5V to V_D and be bypassed to DR GND with a 0.1 µF capacitor. If the supply for this pin is different from the supply used for V_A and V_D, it should also be bypassed with a 10 µF capacitor. V_{DR} should never exceed the voltage on V_D. All bypass capacitors should be located near the supply pin.
30,35,40, 45,50	DRGND	The ground return for the ADC12QS065's output drivers.

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_A, V_D, V_{DR}	3.8V
$\lvert V_A–V_D \rvert$	≤ 100 mV
Voltage on any pin (excludes pins 29 to 45)	−0.3V to (V_A or V_D +0.3V)
Voltage on any pin (pins 29 to 45)	-0.3V to 2V
Input Current at Any Pin (Note 3)	±25 mA
Package Input Current (Note 3)	±50 mA
Package Dissipation at T_A = 25°C	See (Note 4)
ESD Susceptibility	
Human Body Model (Note 5)	2500V
Machine Model (Note 5)	250V
Soldering Temperature, Infrared, 10 sec. (Note 6)	235°C
Storage Temperature	−65°C to +150°C

Soldering process must comply with National Semiconductor's Reflow Temperature Profile specifications. Refer to www.national.com/packaging.

Operating Ratings (Notes 1, 2)

Operating Temperature	−40°C ≤ T_A ≤ +85°C
Supply Voltage (V_A, V_D)	+3.0V to +3.6V
Output Driver Supply (V_{DR})	+2.4V to V_D
V_{IN} Differential Input Range	±V_{REF}
V_{CM} Input Common Mode Range (Differential Input)	V_{REF}/2 to (V_A - V_{REF}/2)
External V_{REF} Voltage Range	0.8V to 1V
Digital Input Pins Voltage Range (excludes pins 31 to 50)	−0.3V to (V_A + 0.3V)
$\lvert$AGND–DGND$\rvert$	≤100mV
Clock Duty Cycle	30% to 70%

Converter Electrical Characteristics

Unless otherwise specified, the following specifications apply for AGND = DGND = DRGND = 0V, V_A = V_D = +3.3V, V_{DR}= +2.5V, Internal V_{REF} = +1.0V, f_{CLK} = 65 MHz, f_{IN} = 5 KHz, C_L = 15 pF/pin. **Boldface limits apply for T_J = T_{MIN} to T_{MAX}:** all other limits T_J = 25°C (Notes 7, 8, 9)

Symbol	Parameter	Conditions		Typical (Note 10)	Limits (Note 10)	Units (Limits)
STATIC CONVERTER CHARACTERISTICS						
	Resolution with No Missing Codes				**12**	Bits (min)
INL	Integral Non Linearity			±0.7	**±1.4**	LSB (max)
DNL	Differential Non Linearity			±0.3	**±0.7**	LSB (max)
PGE	Positive Gain Error			±1.5	**±3.5**	%FS (max)
NGE	Negative Gain Error			±1.1	**±3.5**	%FS (max)
TC GE	Gain Error Tempco	−40°C ≤ T_A ≤ +85°C		7.5		ppm/°C
V_{OFF}	Offset Error (V_{IN}+ = V_{IN}–)			±0.06	**±0.75**	%FS (max)
TC V_{OFF}	Offset Error Tempco	−40°C ≤ T_A ≤ +85°C		4.4		ppm/°C
	Under Range Output Code			0	**0**	
	Over Range Output Code			4095	**4095**	
REFERENCE AND ANALOG INPUT CHARACTERISTICS						
V_{CM}	Common Mode Input Voltage			1.5	**0.5**	V (min)
					2.0	V (max)
V_{IN}	Analog Differential Input Range				**2.0**	V_{P-P}
C_{IN}	V_{IN} Input Capacitance (each pin to GND)	V_{IN} = 2.5 Vdc + 0.7 V_{rms}	(CLK LOW)	8		pF
			(CLK HIGH)	3		pF
V_{REF}	External Reference Voltage (Note 12)			1.00	**0.8**	V (min)
					1	V (max)
	Reference Input Resistance			1		MΩ (min)

Unless otherwise specified, the following specifications apply for AGND = DGND = DRGND = 0V, $V_A = V_D$ = +3.3V, V_{DR}= +2.5V, External V_{REF} = +1.0V, f_{CLK} = 65 MHz, f_{IN} = 5 MHz, C_L = 15 pF/pin. **Boldface limits apply for $T_J = T_{MIN}$ to T_{MAX}:** all other limits T_J = 25°C (Notes 7, 8, 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 10)	Units (Limits)
DYNAMIC CONVERTER CHARACTERISTICS					
FPBW	Full Power Bandwidth	0 dBFS Input, Output at −3 dB	300		MHz
SNR	Signal-to-Noise Ratio (Note 13)	f_{IN} = 5 MHz, V_{IN} = −1 dBFS	69.3	**68.4**	dBFS (min)
		f_{IN} = 33 MHz, V_{IN} = −1 dBFS	68.5		dBFS
SINAD	Signal-to-Noise and Distortion (Note 13)	f_{IN} = 5 MHz, V_{IN} = −1 dBFS	69	**68**	dBFS (min)
		f_{IN} = 33 MHz, V_{IN} = −1 dBFS	68		dBFS
ENOB	Effective Number of Bits (Note 13)	f_{IN} = 5 MHz, V_{IN} = −1 dBFS	11.2	**11**	Bits (min)
		f_{IN} = 33 MHz, V_{IN} = −1 dBFS	11		Bits
THD	Total Harmonic Distortion	f_{IN} = 5 MHz, V_{IN} = −1 dBFS	−82	**-74.5**	dBc (min)
		f_{IN} = 33 MHz, V_{IN} = −1 dBFS	−78		dBc
H2	Second Harmonic Distortion	f_{IN} = 5 MHz, V_{IN} = −1 dBFS	−92.5	**-79**	dBc
		f_{IN} = 33 MHz, V_{IN} = −1 dBFS	−83		dBc
H3	Third Harmonic Distortion	f_{IN} = 5 MHz, V_{IN} = −1 dBFS	−83.3	**-75.5**	dBc
		f_{IN} = 33 MHz, V_{IN} = −1 dBFS	−80		dBc
SFDR	Spurious Free Dynamic Range	f_{IN} = 5 MHz, V_{IN} = −1 dBFS	83.3	**75.5**	dBc
		f_{IN} = 33 MHz, V_{IN} = −1 dBFS	80		dBc
IMD	Intermodulation Distortion	f_{IN} = 19.6 MHz and 20.2 MHz, each = −7 dBFS	−78		dBFS
FPBW	Full Power Bandwidth			300	MHz
INTER-CHANNEL CHARACTERISTICS					
	Channel—Channel Offset Match		±0.3		%FS
	Channel—Channel Gain Match		±4		%FS
	Crosstalk (between any two channels)	10 MHz Tested, Channel; 20 MHz Other Channel	85		dBc

DC and Logic Electrical Characteristics

Unless otherwise specified, the following specifications apply for AGND = DGND = DRGND = 0V, $V_A = V_D = +3.3V$, $V_{DR}= +2.5V$, External $V_{REF} = +1.0V$, $f_{CLK} = 65$ MHz, $f_{IN} = 5$ MHz, $C_L = 15$ pF/pin. **Boldface limits apply for $T_J = T_{MIN}$ to T_{MAX}:** all other limits $T_J = 25°C$ (Notes 7, 8, 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 10)	Units (Limits)
DIGITAL INPUT CHARACTERISTICS					
$V_{IN(1)}$	Logical “1” Input Voltage	$V_D = 3.6V$		**2.0**	V (min)
$V_{IN(0)}$	Logical “0” Input Voltage	$V_D = 3.0V$		**0.5**	V (max)
$I_{IN(1)}$	Logical “1” Input Current	$V_{IN} = 3.3V$	1		µA
$I_{IN(0)}$	Logical “0” Input Current	$V_{IN} = 0V$	−1		µA
POWER SUPPLY CHARACTERISTICS					
I_A	Analog Supply Current	PD Pin = DGND PD Pin = V_D	168 0.5	**200**	mA (max) mA
I_D	Digital Supply Current	PD Pin = DGND PD Pin = V_D	48 0.2	**53**	mA (max) mA
I_{DR}	LVDS Output Supply Current	PD Pin = DGND, $f_{IN} = 33$ MHz	46	**62**	mA (max)
PWR	Total Power Consumption (includes driver supply)	PD Pin = DGND, $C_L = 5$ pF PD Pin = V_D	828 3	**990**	mW (max) mW
PSRR	Power Supply Rejection Ratio	Rejection of Full-Scale Error with $V_A = 3.0V$ vs. 3.6V	53		dB

AC Electrical Characteristics

Unless otherwise specified, the following specifications apply for AGND = DGND = DRGND = 0V, $V_A = V_D = +3.3V$, $V_{DR}= +2.5V$, External $V_{REF} = +1.0V$, $f_{CLK} = 65$ MHz, $f_{IN} = 5$ MHz, $C_L = 15$ pF/pin. **Boldface limits apply for $T_J = T_{MIN}$ to T_{MAX}:** all other limits $T_J = 25°C$ (Notes 7, 8, 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 10)	Units (Limits)
f_{CLK1}	Maximum Clock Frequency			**65**	MHz (min)
f_{CLK2}	Minimum Clock Frequency		20		MHz
	Clock Duty Cycle		50	30 70	% min % max
t_{CONV}	Conversion Latency	Input Sample(N) to LSB of Sample(N) Data valid		**9**	Clock Cycles
t_{AD}	Aperture Delay		2		ns
t_{AJ}	Aperture Jitter		1		ps rms
t_{PD}	Power Down Mode Exit Cycle		<5		ms

LVDS Electrical Characteristics

Unless otherwise specified, the following specifications apply for AGND = DGND = DRGND = 0V, $V_A = V_D = +3.3V$, $V_{DR}= +2.5V$, External $V_{REF} = +1.0V$, $f_{CLK} = 65$ MHz, $f_{IN} = 5$ MHz, $C_L = 15$ pF/pin. **Boldface limits apply for $T_J = T_{MIN}$ to T_{MAX}:** all other limits $T_J = 25°C$ (Notes 7, 8, 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 10)	Units (Limits)
LVDS DC CHARACTERISTICS					
V_{OD}	Output Differential Voltage (DO+) - (DO-)	$R_L = 100\Omega$	290	230 450	mV (min) mV (max)
delta V_{OD}	Output Differential Voltage Unbalance	$R_L = 100\Omega$	±1	±15	mV (max)
V_{OS}	Offset Voltage	$R_L = 100\Omega$	1.25	1.125 1.375	V (min) V (max)
delta V_{OS}	Offset Voltage Unbalance	$R_L = 100\Omega$	±7	±25	mV (max)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 10)	Units (Limits)
IOS	Output Short Circuit Current	DO = 0V, V_{IN} = 1.1V,	-10		mA (max)
LVDS OUTPUT TIMING AND SWITCHING CHARACTERISTICS					
t_{OCP}	Output Clock Period	50% to 50%	2.56		ns
t_{OCDC}	Output Clock Duty Cycle	(Note 14)	50	35 65	% (min) % (max)
t_H	Data Edge to Output Clock Edge Hold Time	50% to 50% (Note 14)	625	300	ps
t_S	Data Edge to Output Clock Edge Set-Up Time	50% to 50% (Note 14)	600	300	ps
t_{FP}	Frame Period	50% to 50%	15.38		ns
t_{FDC}	Frame Clock Duty Cycle	(Note 14)	50	45 55	% (min) % (max)
t_{DFS}	Data Edge to Frame Edge Skew	50% to 50%	60	160	ps (max)
t_R, t_F	LVDS Rise/Fall Time	C_L=5pF to GND, R_{OUT}=100Ω	360	700	ps (max)
t_{PLD}	Serializer PLL Lock Time		50		µs
t_{SD}	Serializer Delay	R_L=100Ω	2.76		ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is guaranteed to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the maximum Operating Ratings is not recommended.

Note 2: All voltages are measured with respect to GND = AGND = DGND = 0V, unless otherwise specified.

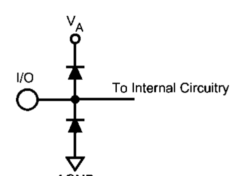
Note 3: When the input voltage at any pin exceeds the power supplies (that is, V_{IN} < AGND, or V_{IN} > V_A), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two.

Note 4: The absolute maximum junction temperature ($T_J$max) for this device is 150°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature, (T_A), and can be calculated using the formula P_DMAX = ($T_J$max - T_A)/θ_{JA}. In the 60-pin LLP, θ_{JA} is 20°C/W with the exposed pad soldered to a ground plane, so P_DMAX = 2 W at the maximum operating ambient temperature of 85°C. Note that the power consumption of this device under normal operation will typically be about 900 mW. The values for maximum power dissipation listed above will be reached only when the device is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.

Note 5: Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through 0Ω.

Note 6: Reflow Reflow temperature profiles are different for lead-free and non-lead-free packages.

Note 7: The inputs are protected as shown below. Input voltage magnitudes above V_A or below GND will not damage this device, provided current is limited per (Note 3). However, errors in the A/D conversion can occur if the input goes above V_A or below GND by more than 100 mV. As an example, if V_A is +3.3V, the full-scale input voltage must be ≤+3.4V to ensure accurate conversions.



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Note 8: To guarantee accuracy, it is required that $|V_A–V_D| \leq$ 100 mV and separate bypass capacitors are used at each power supply pin.

Note 9: With the test condition for V_{REF} = +1.0V ($2V_{P-P}$ differential input), the 12-bit LSB is 488 µV.

Note 10: Typical figures are at T_A = 25°C, and represent most likely parametric norms at the time of product characterization. The typical specifications are not guaranteed.

Note 11: Timing specifications are tested at TTL logic levels, V_{IL} = 0.4V for a falling edge and V_{IH} = 2.0V for a rising edge.

Note 12: Optimum performance will be obtained by keeping the reference input in the 0.8V to 1V range. The LM4051CIM3-ADJ (SOT-23 package) is recommended for external reference applications.

Note 13: This parameter is specified in dBFS - indicating the value that would be attained with a full-scale input signal.

Note 14: This parameter is guaranteed by design and/or qualification and is not tested in production.

Specification Definitions

APERTURE DELAY is the time after the rising edge of the clock to when the input signal is acquired or held for conversion.

APERTURE JITTER (APERTURE UNCERTAINTY) is the variation in aperture delay from sample to sample. Aperture jitter manifests itself as noise in the output.

CLOCK DUTY CYCLE is the ratio of the time during one cycle that a repetitive digital waveform is high to the total time of one period. The specification here refers to the ADC clock input signal.

COMMON MODE VOLTAGE (V_{CM}) is the common d.c. voltage applied to both input terminals of the ADC.

CONVERSION LATENCY is the number of clock cycles between initiation of conversion and when that data is presented to the output driver stage. Data for any given sample is available at the output pins the Pipeline Delay plus the Output Delay after the sample is taken. New data is available at every clock cycle, but the data lags the conversion by the pipeline delay.

CROSSTALK is coupling of energy from one channel into the other channel.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as (SINAD - 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It can be calculated as:

Gain Error = Positive Full Scale Error – Negative Full Scale Error

Gain Error can also be separated into Positive Gain Error and Negative Gain Error, which are:

PGE = Positive Full Scale Error – Offset Error

NGE = Offset Error – Negative Full Scale Error

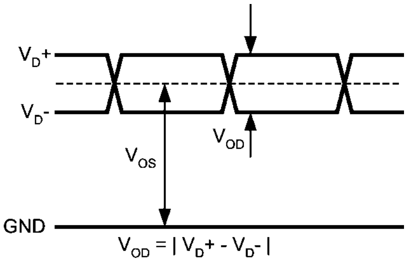
GAIN ERROR MATCHING is the difference in gain errors between the two converters divided by the average gain of the converters.

INTEGRAL NON LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from negative full scale (½ LSB below the first code transition) through positive full scale (½ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the intermodulation products to the total power in the original frequencies. IMD is usually expressed in dBFS.

LSB (LEAST SIGNIFICANT BIT) is the bit that has the smallest value or weight of all bits. This value is $V_{REF}/2^n$, where "n" is the ADC resolution in bits, which is 12 in the case of the ADC12QS065.

LVDS Differential Output Voltage (V_{OD}) is the absolute value of the difference between the differential output pair voltages (V_D+ and V_D-), each measured with respect to ground.



LVDS Output Offset Voltage (V_{OS}) is the midpoint between the differential output pair voltages.

MISSING CODES are those output codes that will never appear at the ADC outputs. The ADC12QS065 is guaranteed not to have any missing codes.

MSB (MOST SIGNIFICANT BIT) is the bit that has the largest value or weight. Its value is one half of full scale.

NEGATIVE FULL SCALE ERROR is the difference between the actual first code transition and its ideal value of ½ LSB above negative full scale.

OFFSET ERROR is the difference between the two input voltages [(V_{IN}+) – (V_{IN-})] required to cause a transition from code 2047 to 2048.

OUTPUT DELAY is the time delay after the rising edge of the clock before the data update is presented at the output pins.

OVER RANGE RECOVERY TIME is the time required after V_{IN} goes from a specified voltage out of the normal input range to a specified voltage within the normal input range and the converter makes a conversion with its rated accuracy.

PIPELINE DELAY (LATENCY) See CONVERSION LATENCY.

POSITIVE FULL SCALE ERROR is the difference between the actual last code transition and its ideal value of 1½ LSB below positive full scale.

POWER SUPPLY REJECTION RATIO (PSRR) is a measure of how well the ADC rejects a change in the power supply voltage. For the ADC12QS065, PSRR is the ratio of the change in Full-Scale Error that results from a change in the d.c. power supply voltage, expressed in dB.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or d.c.

SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD) Is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the desired signal amplitude to the amplitude of the peak spurious spectral component, where a spurious spectral component is any signal present in the output spectrum that is not present at the input and may or may not be a harmonic.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dB, of the rms total of the first nine harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

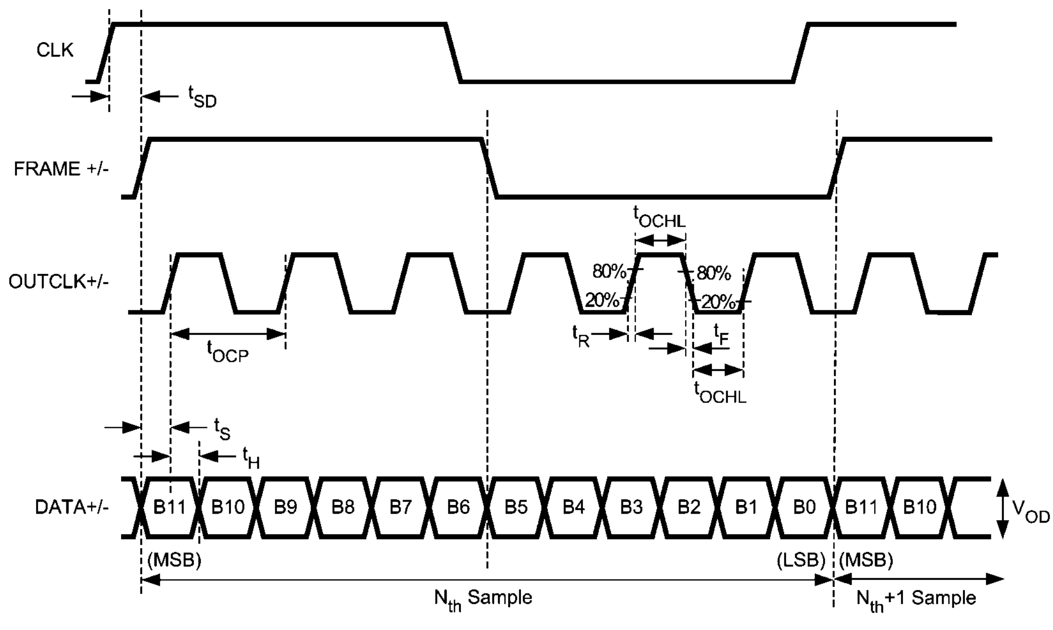
$$THD = 20 \times \log \sqrt{\frac{A_{f2}^2 + \ldots + A_{f10}^2}{A_{f1}^2}}$$

where f_1 is the RMS power of the fundamental (output) frequency and f_2 through f_{10} are the RMS power of the first 9 harmonic frequencies in the output spectrum.

SECOND HARMONIC DISTORTION (2ND HARM) is the difference expressed in dB, between the RMS power in the input frequency at the output and the power in its 2nd harmonic level at the output.

THIRD HARMONIC DISTORTION (3RD HARM) is the difference, expressed in dB, between the RMS power in the input frequency at the output and the power in its 3rd harmonic level at the output.

Timing Diagram



LVDS Output Timing

Transfer Characteristic

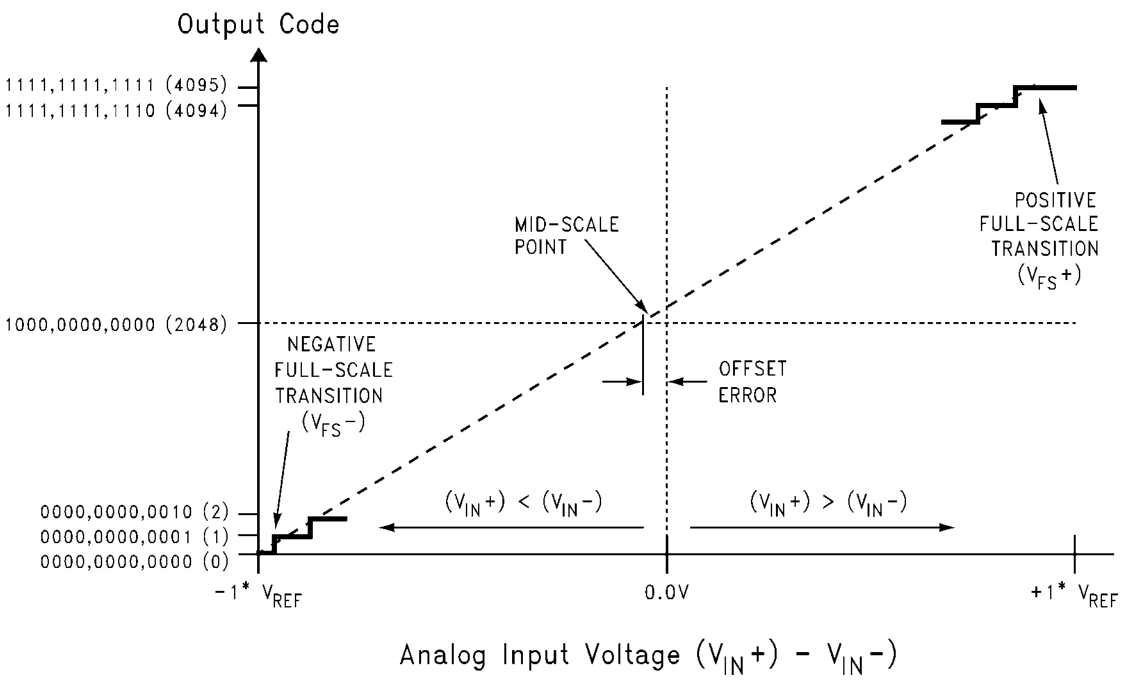
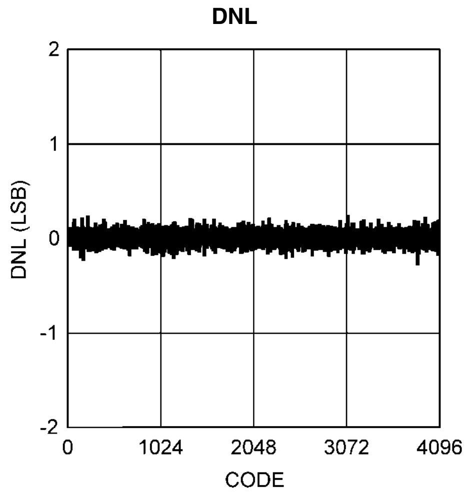


FIGURE 1. Transfer Characteristic

Typical Performance Characteristics DNL, INL

Unless otherwise specified, the following specifications apply for AGND = DGND = DRGND = 0V, $V_A = V_D = +3.3V$, $V_{DR} = +2.5V$, Internal $V_{REF} = +1.0V$, $f_{CLK} = 65$ MHz, $f_{IN} = 5$ KHz, $C_L = 15$ pF/pin.



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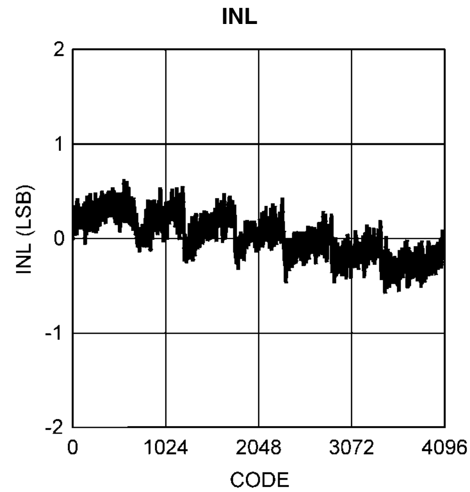

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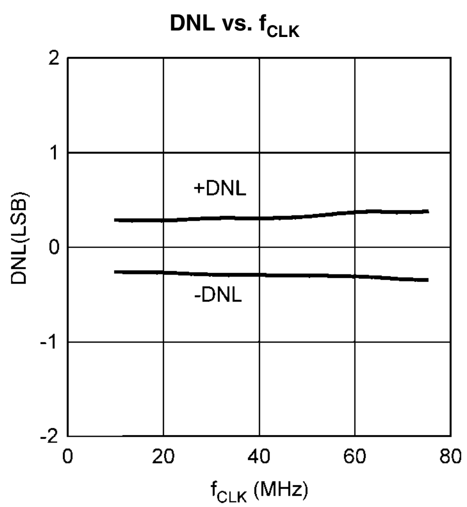

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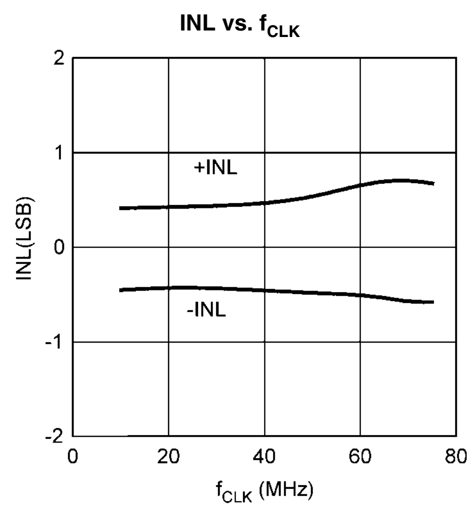

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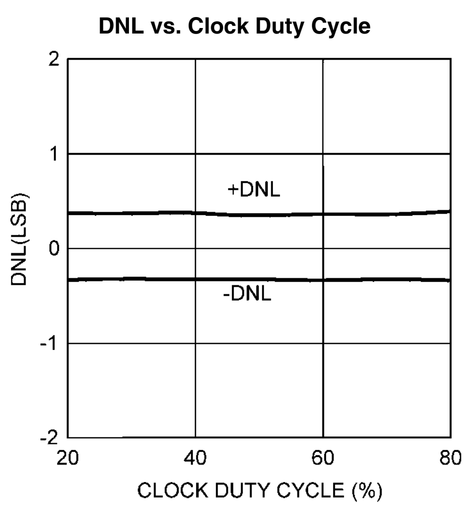

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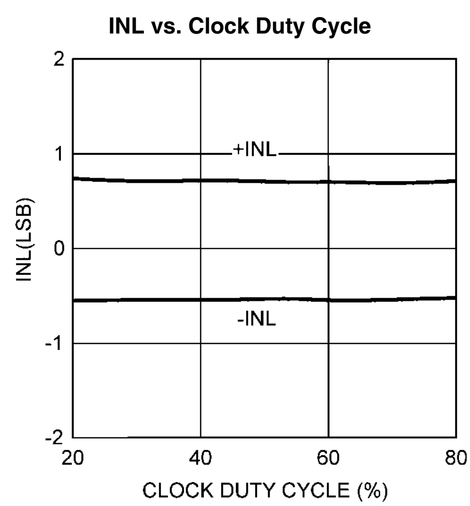

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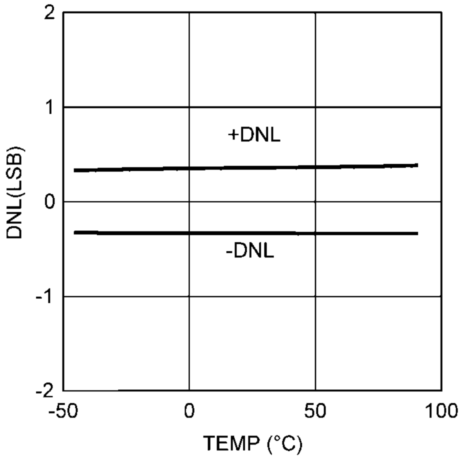
DNL vs. Temperature



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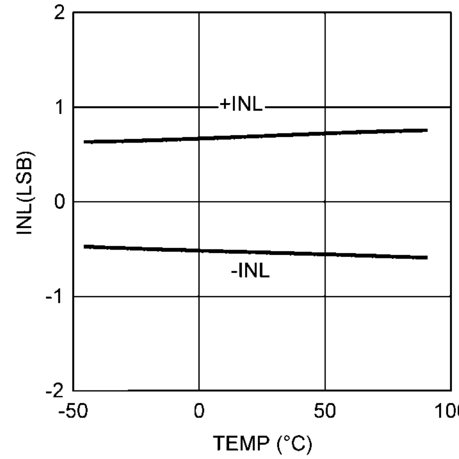
INL vs. Temperature



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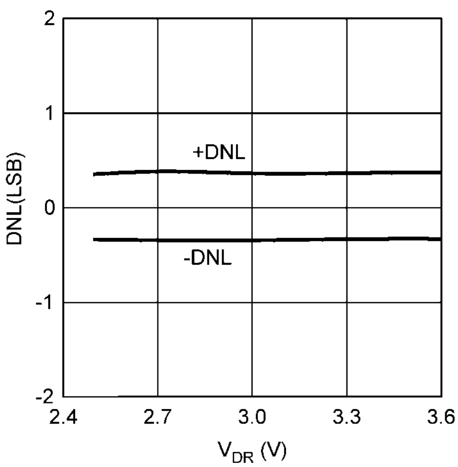
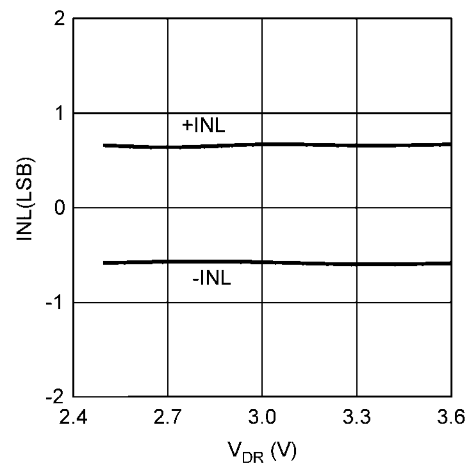
DNL vs. V_{DR}, $V_A = V_D = 3.6V$



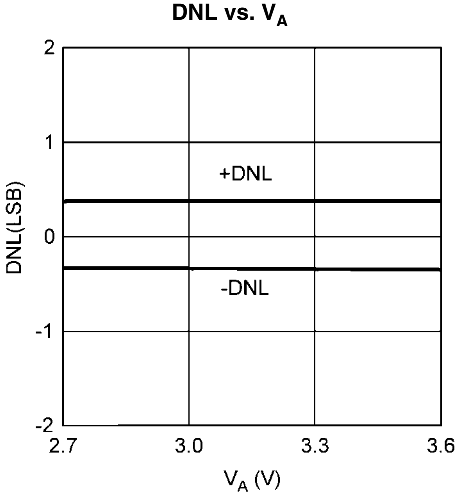
20106839

INL vs. V_{DR}, $V_A = V_D = 3.6V$



20106840

DNL vs. V_A



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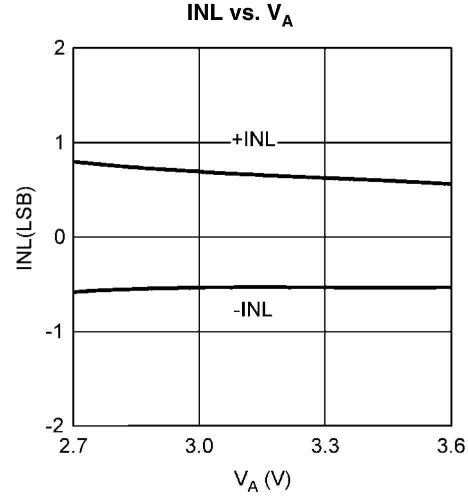
INL vs. V_A

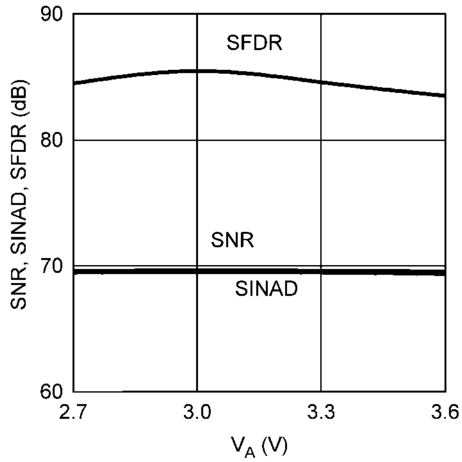


20106842

Typical Performance Characteristics

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, $V_A = V_D = +3.3V$, $V_{DR} = +2.5V$, PD = 0V, External $V_{REF} = +1.0V$, $f_{CLK} = 65$ MHz, $f_{IN} = 5$ MHz, $C_L = 15$ pF/pin. Units for SNR and SINAD are dBFS. Units for SFDR and Distortion are dBc.

SNR, SINAD, SFDR vs. V_A



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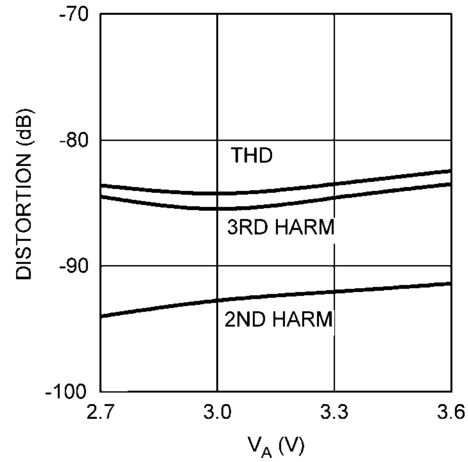
Distortion vs. V_A



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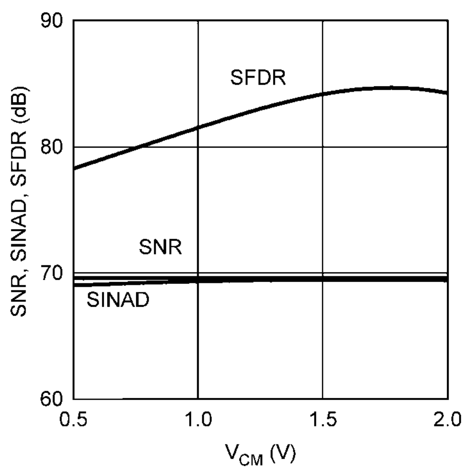
SNR, SINAD, SFDR vs. V_{CM}



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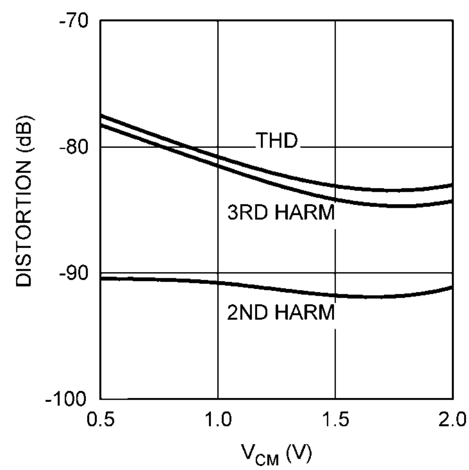
Distortion vs. V_{CM}



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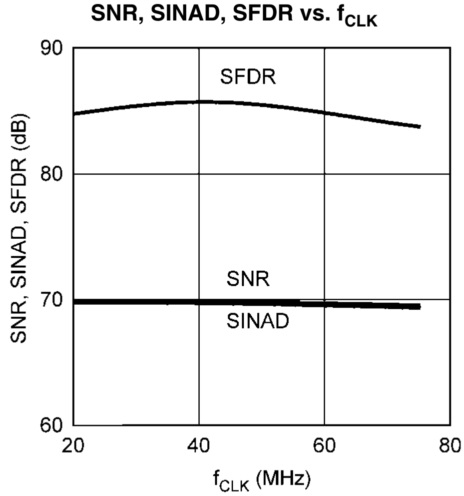
SNR, SINAD, SFDR vs. f_{CLK}



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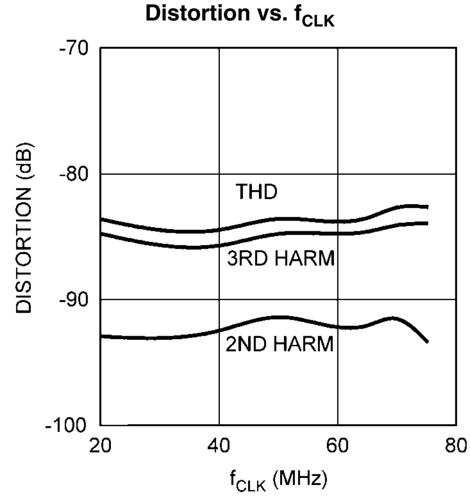
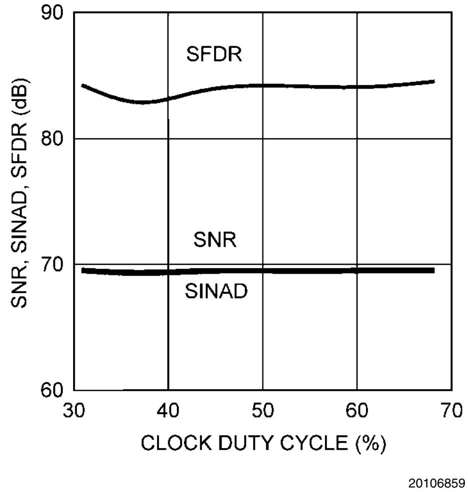
Distortion vs. f_{CLK}

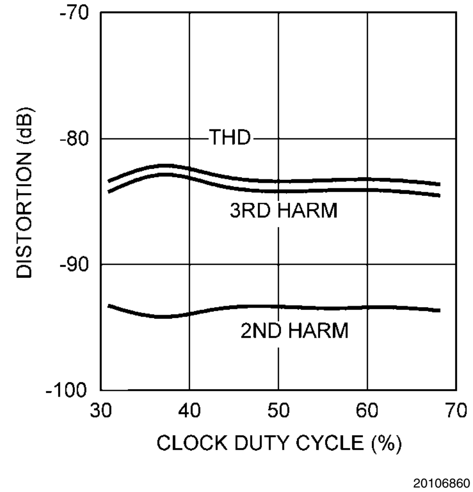


20106858

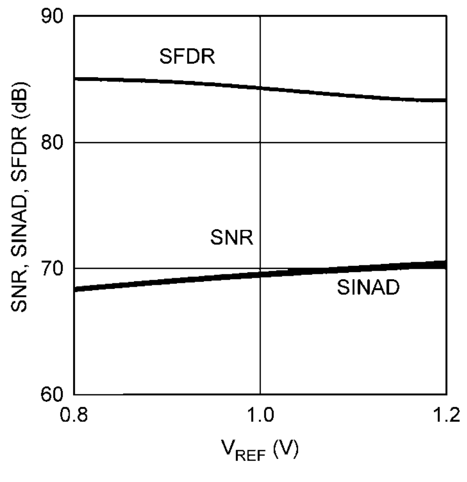
SNR, SINAD, SFDR vs. Clock Duty Cycle



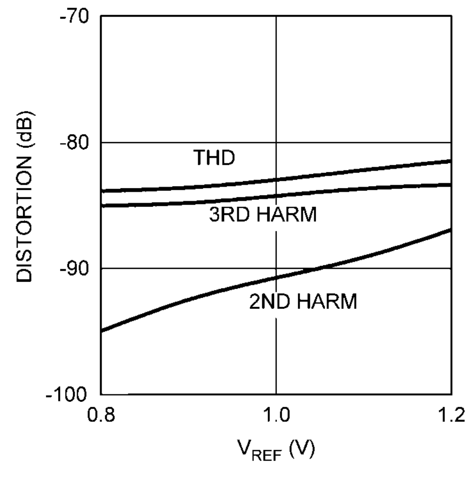
Distortion vs. Clock Duty Cycle



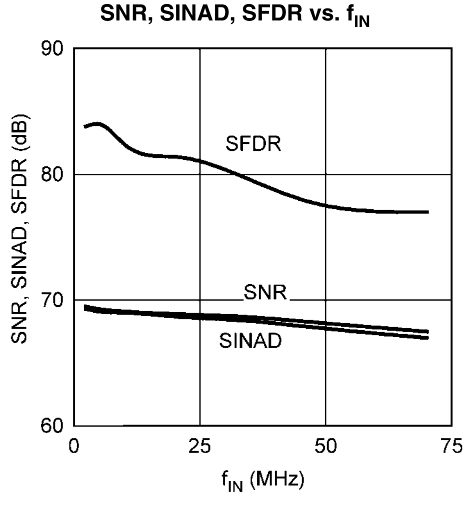
SNR, SINAD, SFDR vs. V_{REF}



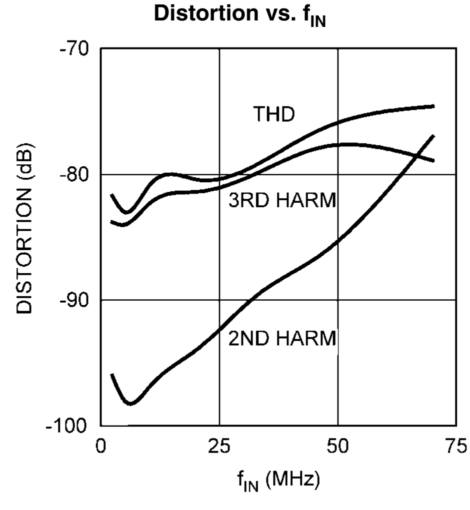
Distortion vs. V_{REF}



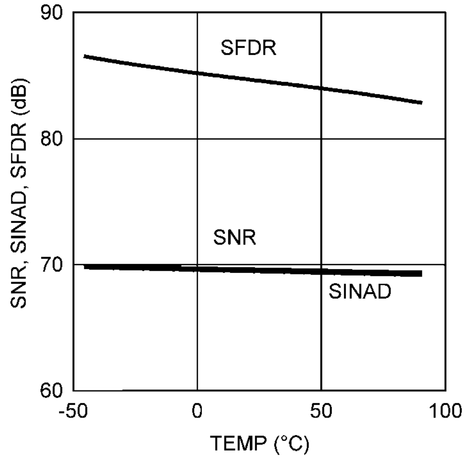
SNR, SINAD, SFDR vs. f_{IN}



Distortion vs. f_{IN}

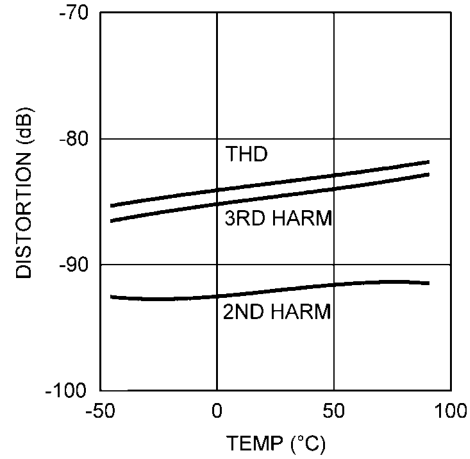


SNR, SINAD, SFDR vs. Temperature



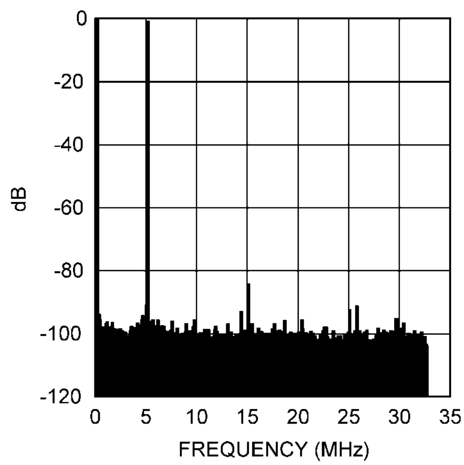
20106865

Distortion vs. Temperature



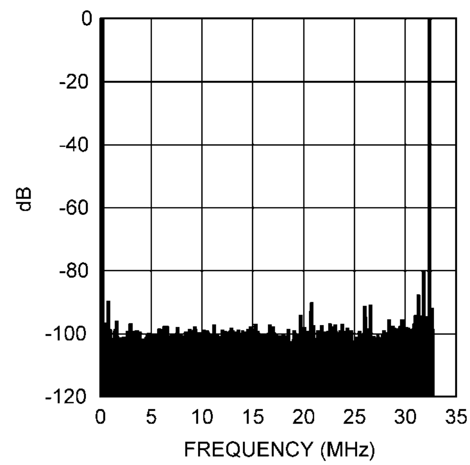
20106866

Spectral Response @ 5 MHz Input



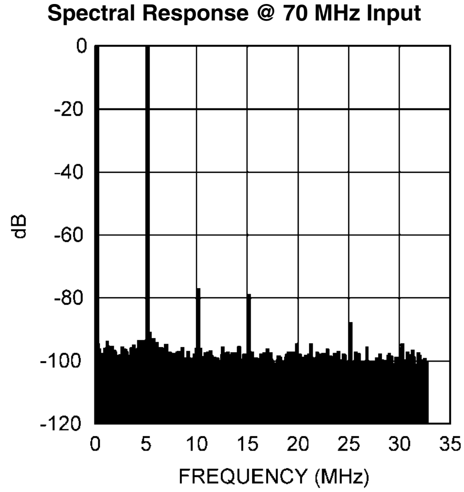
20106871

Spectral Response @ 33 MHz Input



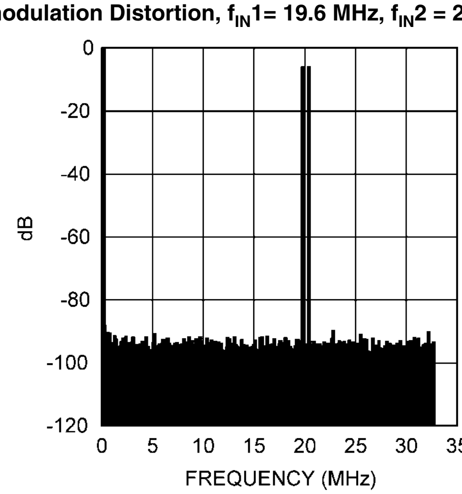
20106872

Spectral Response @ 70 MHz Input



20106873

Intermodulation Distortion, $f_{IN}1$= 19.6 MHz, $f_{IN}2$ = 20.2 MHz



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Functional Description

Operating on a single +3.3V supply, the ADC12QS065 uses a pipeline architecture and has error correction circuitry to help ensure maximum performance. The differential analog input signal is digitized to 12 bits. The user has the choice of using an internal 1.0 Volt or 0.5 Volt stable reference, or using an external reference. Any external reference is buffered on-chip to ease the task of driving that pin.

Sampled data is transformed into high speed serial output LVDS data streams. Clock and frame LVDS pairs aid in data capture. The ADC12QS065's six differential pairs transmit data over backplanes or cable and also make PCB design easier.

The output word rate is the same as the clock frequency, which can be between 20 MSPS and 65 MSPS (typical) with fully specified performance at 65 MSPS. The analog input for all channels are acquired at the rising edge of the clock and the digital data for a given sample is delayed by the pipeline for 9 clock cycles.

Applications Information

1.0 OPERATING CONDITIONS

We recommend that the following conditions be observed for operation of the ADC12QS065:

$3.0V \leq V_A \leq 3.6V$

$V_D = V_A$

$V_{DR = 2.5V}$

$20\ MHz \leq f_{CLK} \leq 65\ MHz$

$0.8V \leq V_{REF} \leq 1V$ (for an external reference)

$0.5V \leq V_{CM} \leq 2.0V$

2.0 ANALOG INPUTS

There is one reference input pin, V_{REF}, which is used to select an internal reference, or to supply an external reference. The ADC12QS065 has four analog signal input pairs, V_{IN} 1+ and V_{IN} 1-, V_{IN} 2+ and V_{IN} 2- , V_{IN} 3+ and V_{IN} 3-, V_{IN} 4+ and V_{IN} 4- . Each pair of pins forms a differential input pair. There is a VREG pin for decoupling the internal 1.8V regulator.

2.1 Reference Pins

The ADC12QS065 is designed to operate with an internal 1.0V or 0.5V reference, or an external 1.0V reference, but performs well with external reference voltages in the range of 0.8V to 1V. Lower reference voltages will decrease the signal-to-noise ratio (SNR) of the ADC12QS065. Increasing the reference voltage (and the input signal swing) beyond 1V may degrade THD for a full-scale input, especially at higher input frequencies.

It is important that all grounds associated with the reference voltage and the analog input signal make connection to the ground plane at a single, quiet point to minimize the effects of noise currents in the ground path.

The six Reference Bypass Pins (VREFT12, VREFB12, VCOM12, VREFT34, VREFB34 and VCOM34) are made available for bypass purposes. All these pins should each be bypassed to ground with a 0.1 µF capacitor. A 10 µF capacitor should be placed between the VREFT12 and VREFB12 pins and between the VREFT34 and VREFB34 pins, as shown in *Figure 4*. This configuration is necessary to avoid reference oscillation, which could result in reduced SFDR and/or SNR.

Smaller capacitor values than those specified will allow faster recovery from the power down mode, but may result in degraded noise performance.

The VCOM pins may be loaded to 1 mA. The remaining reference bypass pins should not be loaded.

The nominal voltages for the reference bypass pins are as follows:

VCOM = 1.5 V

$VREFT = VCOM + V_{REF} / 2$

$VREFB = VCOM - V_{REF} / 2$

User choice of an on-chip or external reference voltage is provided. When INTREF is high, the V_{REF} pin selects the internal reference voltage. The internal 1.0 Volt reference is in use when the the V_{REF} pin is connected to V_A. When the V_{REF} pin is connected to AGND, the internal 0.5 Volt reference is in use. When INTREF is low, a voltage in the range of 0.8V to 1V is applied to the V_{REF} pin and that is used for the voltage reference. When an external reference is used, the V_{REF} pin should be bypassed to ground with a 0.1 µF capacitor close to the reference input pin. There is no need to bypass the V_{REF} pin when the internal reference is used.

2.2 Signal Inputs

The ADC12QS065 has 4 input channels. They are labelled V_{IN} 1+ and V_{IN}1– , V_{IN} 2+ and V_{IN}2– , V_{IN} 3+ and V_{IN}3– , V_{IN} 4+ and V_{IN}4– . The input signal, V_{IN}, is defined as

$$V_{IN} = (V_{IN}+) - (V_{IN}-)$$

Figure 2 shows the expected input signal range. Note that the common mode input voltage, V_{CM}, should be in the range of 0.5V to 2.0V with a typical value of 1.5V.

The peaks of the individual input signals should each never exceed 2.6V to maintain THD and SINAD performance.

The ADC12QS065 performs best with a differential input signal with each input centered around a common mode voltage, V_{CM}. The peak-to-peak voltage swing at each analog input pin should not exceed the value of the reference voltage or the output data will be clipped.

The two input signals should be exactly 180° out of phase from each other and of the same amplitude. For single frequency inputs, angular errors result in a reduction of the effective full scale input. For complex waveforms, however, angular errors will result in distortion.

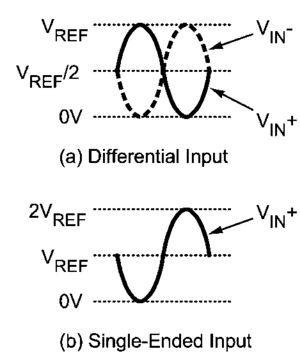


FIGURE 2. Expected Input Signal Range

For single frequency sine waves the full scale error in LSB can be described as approximately

$$E_{FS} = 4096\ (\ 1 - \sin\ (90° + dev))$$

Where dev is the angular difference in degrees between the two signals having a 180° relative phase relationship to each other (see *Figure 3*). Drive the analog inputs with a source impedance less than 100Ω.

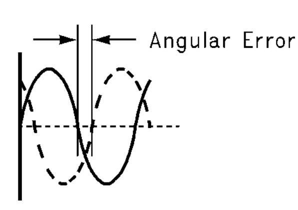


FIGURE 3. Angular Errors Between the Two Input Signals Will Reduce the Output Level or Cause Distortion

For differential operation, each analog input pin of the differential pair should have a peak-to-peak voltage just below the reference voltage, V_{REF}, be 180 degrees out of phase with each other and be centered around V_{CM}.

2.2.1 Single-Ended Operation

Performance with differential input signals is better than with single-ended signals. For this reason, single-ended operation is not recommended. However, if single ended-operation is required and the resulting performance degradation is acceptable, one of the analog inputs should be connected to the d.c. mid point voltage of the driven input. The peak-to-peak differential input signal at the driven input pin should be twice the reference voltage to maximize SNR and SINAD performance (*Figure 2b*). For example, set V_{REF} to 0.5V, bias $V_{IN}-$ to 1.0V and drive $V_{IN}+$ with a signal range of 0.5V to 1.5V.

Because very large input signal swings can degrade distortion performance, better performance with a single-ended input can be obtained by reducing the reference voltage when maintaining a full-range output. *Table 1* and *Table 2* indicate the input to output relationship of the ADC12QS065.

TABLE 1. Input to Output Relationship – Differential Input

V_{IN+}	V_{IN-}	Binary Output
$V_{CM} - V_{REF}/2$	$V_{CM} + V_{REF/2}$	0000 0000 0000
$V_{CM} - V_{REF/4}$	$V_{CM} + V_{REF}/4$	0100 0000 0000
V_{CM}	V_{CM}	1000 0000 0000
$V_{CM} + V_{REF}/4$	$V_{CM} - V_{REF}/4$	1100 0000 0000
$V_{CM} + V_{REF}/2$	$V_{CM} - V_{REF}/2$	1111 1111 1111

TABLE 2. Input to Output Relationship – Single-Ended Input

V_{IN+}	V_{IN-}	Binary Output
$V_{CM} - V_{REF}$	V_{CM}	0000 0000 0000
$V_{CM} - V_{REF}/2$	V_{CM}	0100 0000 0000
V_{CM}	V_{CM}	1000 0000 0000
$V_{CM} + V_{REF}/2$	V_{CM}	1100 0000 0000
$V_{CM} + V_{REF}$	V_{CM}	1111 1111 1111

2.2.2 Driving the Analog Inputs

The $V_{IN}+$ and the $V_{IN}-$ inputs of the ADC12QS065 consist of an analog switch followed by a switched-capacitor amplifier. As the internal sampling switch opens and closes, current pulses occur at the analog input pins, resulting in voltage spikes at the signal input pins. As a driving source attempts to counteract these voltage spikes, it may add noise to the signal at the ADC analog input. To help isolate the pulses at the ADC input from the amplifier output, use RCs at the inputs, as can be seen in *Figure 4* and *Figure 5*. These components should be placed close to the ADC inputs because the input pins of the ADC is the most sensitive part of the system and this is the last opportunity to filter that input.

For Nyquist applications the RC pole should be at the ADC sample rate. The ADC input capacitance in the sample mode should be considered when setting the RC pole. For wideband undersampling applications, the RC pole should be set at about 1.5 to 2 times the maximum input frequency to maintain a linear delay response.

2.2.3 Input Common Mode Voltage

The input common mode voltage, V_{CM}, should be in the range of 0.5V to 2.0V and be a value such that the peak excursions of the analog signal does not go more negative than ground or more positive than 2.6V. The nominal V_{CM} should generally be about 1.5V. VCOM12 or VCOM34 can be used as a V_{CM} source.

2.3 Internal Regulator

The ADC12QS065 has an internal 1.8V regulator. The VREG pin (pin 29) should be bypassed to AGND with a 1.0 µF capacitor.

3.0 DIGITAL INPUTS

Digital TTL/CMOS compatible inputs consist of CLK, PD, REFPD, and INTREF.

3.1 CLK

The **CLK** signal controls the timing of the sampling process. Drive the clock input with a stable, low jitter clock signal in the range of 20 MHz to 65 MHz. The trace carrying the clock signal should be as short as possible and should not cross any other signal line, analog or digital, not even at 90°.

The **CLK** signal also drives an internal state machine. If the **CLK** is interrupted, or its frequency too low, the charge on internal capacitors can dissipate to the point where the accuracy of the output data will degrade. This is what limits the minimum sample rate.

The ADC12QS065 can operate with a CMOS or LVDS clock signal.

For a CMOS clock, connect CLKB (pin 48) to AGND and apply the clock signal to CLK (pin 47.) The clock line should be terminated at its source in the characteristic impedance of that line. Take care to maintain a constant clock line impedance throughout the length of the line. Refer to Application Note AN-905 for information on setting characteristic impedance. It is highly desirable that the the source driving the ADC **CLK** pin only drive that pin. However, if that source is used to drive other things, each driven pin should be a.c. terminated with a series RC to ground, such that the resistor value is equal to the characteristic impedance of the clock line and the capacitor value is

$$C \geq \frac{4 \times t_{PD} \times L}{Z_o}$$

where t_{PD} is the signal propagation rate down the clock line, "L" is the line length and Z_O is the characteristic impedance of the clock line. This termination should be as close as possible to the ADC clock pin but beyond it as seen from the clock source. Typical t_{PD} is about 150 ps/inch (60 ps/cm) on FR-4 board material. The units of "L" and t_{PD} should be the same (inches or centimeters).

For an LVDS clock, drive the CLK and CLKB pins with an ac-coupled differential clock signal. The pair should be terminated with a 100Ω resistor near the pins.

3.2 PD

The PD pin, when high, holds the ADC12QS065 in a power-down mode to conserve power when the converter is not being used. The power consumption in this state is 3 mW with a 65MHz clock.. The output data pins are undefined and the data in the pipeline is corrupted while in the power down mode.

The Power Down Mode Exit Cycle time is determined by the value of the components on the reference bypass pins 55-57, and 20-22, and is as listed in the Electrical Tables with the recommended components on the VREFT, VREFB and VCOM reference bypass pins. These capacitors loose their charge in the Power Down mode and must be recharged by on-chip circuitry before conversions can be accurate. Smaller capacitor values allow slightly faster recovery from the power down mode, but can result in a reduction in SNR, SINAD and ENOB performance.

3.3 REFPD

When high, the REFPD pin will power down the internal reference. With REFPD high, user must drive VREFT12, VREFT34 and VREFB12 & VREFB34 externally. With REFPD low, VREFT12, VREFT34, VREFB12 and VREFB34 are driven internally.

3.4 INTREF

When INTREF is connected to V_D , two internal reference choices are selectable through the V_{REF} pin (pin 23). When INTREF is connected to DGND, an external reference must be applied to V_{REF}.*2.1 Reference Pins*

4.0 OUTPUTS

The ADC12QS065 has four Low Voltage Differential Signaling (LVDS) Data Output pairs. Valid data is present at these outputs while the PD pin is low. The OUTCLK and FRAME pins aid in data capture.

LVDS signals provide a high level of immunity to common mode noise. The differential data signals consist of two 350mVpp (typical) signals that are 180 degrees out of phase. The PCB traces for these signals should be treated as transmission lines. Each signal pair should have closely coupled traces designed with 100Ω differential impedance and should be terminated with a 100Ω resistor near the receiver.

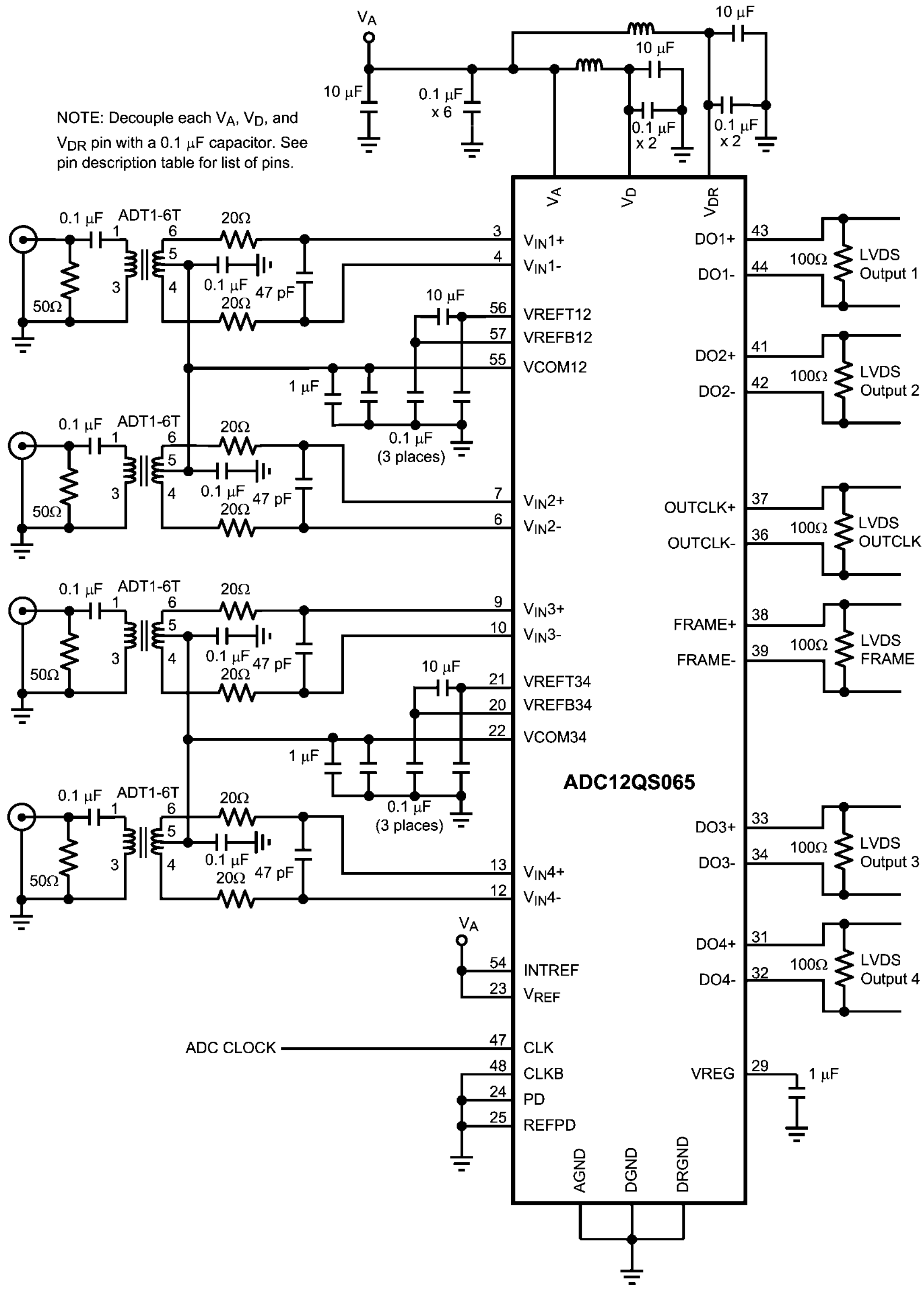


FIGURE 4. Application Circuit using Transformer Drive Circuit

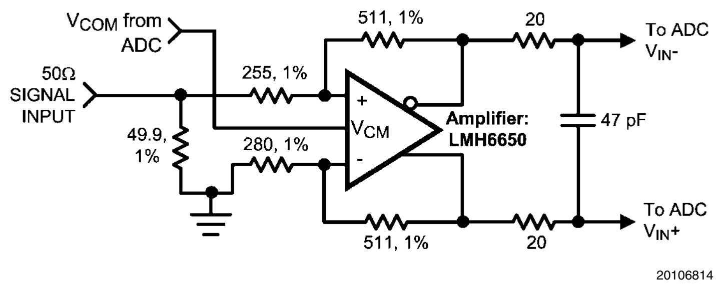


FIGURE 5. Differential Op-Amp Drive Circuit of *Figure 4*

5.0 POWER SUPPLY CONSIDERATIONS

The power supply pins should be bypassed with a 10 µF capacitor and with a 0.1 µF ceramic chip capacitor close to each power pin. Leadless chip capacitors are preferred because they have low series inductance.

As is the case with all high-speed converters, the ADC12QS065 is sensitive to power supply noise. Accordingly, the noise on the analog supply pin should be kept below 100 mV_{P-P}.

No pin should ever have a voltage on it that is in excess of the supply voltages, not even on a transient basis. Be especially careful of this during power turn on and turn off.

6.0 LAYOUT AND GROUNDING

Proper grounding and proper routing of all signals are essential to ensure accurate conversion. Maintaining separate analog and digital areas of the board, with the ADC12QS065 between these areas, is required to achieve specified performance.

The package of the ADC12QS065 has an exposed pad on its back that provides the primary heat removal path as well as electrical grounding to the printed circuit board. The exposed pad must be attached to the board to remove the maximum amount of heat from the package, as well as to ensure best product parametric performance.

To maximize the removal of heat from the package, a thermal land pattern must be incorporated on the PC board within the footprint of the package. The land pattern for this exposed pad should be at least as large as the exposed pad of the package and be located such that the exposed pad of the device is entirely over that thermal land pattern. This thermal land pattern should be electrically connected to ground.

To minimize junction temperature, it is recommended that a simple heat sink be built into the PCB. This is done by including a copper area on the opposite side of the PCB. This copper area may be plated or solder coated to prevent corrosion, but should not have a conformal coating, which could provide some thermal insulation. Thermal vias should be used to connect these top and bottom copper areas. These thermal vias act as "heat pipes" to carry the thermal energy from the device side of the board to the opposite side of the board where it can be more effectively dissipated. The use of 9 to 16 thermal vias is recommended. The thermal vias should be placed on a 1.2 mm grid spacing and have a diameter of 0.30 to 0.33 mm. These vias should be barrel plated to avoid solder wicking into the vias during the soldering process.

The ground return for the data outputs (DRGND) carries the ground current for the output drivers. The output current can exhibit high transients that could add noise to the conversion process. To prevent this from happening, the DRGND pins should NOT be connected to system ground in close proximity to any of the ADC12QS065's other ground pins.

Capacitive coupling between the typically noisy digital circuitry and the sensitive analog circuitry can lead to poor performance. The solution is to keep the analog circuitry separated from the digital circuitry, and to keep the clock line as short as possible.

The LVDS output pairs should be routed with a 100Ω differential impedance trace, and should be terminated at the receiver with a 100Ω resistor.

Since digital switching transients are composed largely of high frequency components, total ground plane copper weight will have little effect upon the logic-generated noise. This is because of the skin effect. Total surface area is more important than is total ground plane volume.

Generally, analog and digital lines should cross each other at 90° to avoid crosstalk. To maximize accuracy in high speed, high resolution systems, however, avoid crossing analog and digital lines altogether. It is important to keep clock lines as short as possible and isolated from ALL other lines, including other digital lines. Even the generally accepted 90° crossing should be avoided with the clock line as even a little coupling can cause problems at high frequencies. This is because other lines can introduce jitter into the clock line, which can lead to degradation of SNR. Also, the high speed clock can introduce noise into the analog chain.

Best performance at high frequencies and at high resolution is obtained with a straight signal path. That is, the signal path through all components should form a straight line wherever possible.

Be especially careful with the layout of inductors. Mutual inductance can change the characteristics of the circuit in which they are used. Inductors should *not* be placed side by side, even with just a small part of their bodies beside each other.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input pins and ground or to the reference input pin and ground should be connected to a very clean point in the ground plane. Traces for the input channels should be routed away from each other as much as possible, with Ground plane between channels, to help minimize crosstalk.

7.0 DYNAMIC PERFORMANCE

To achieve the best dynamic performance, the clock source driving the CLK input must be free of jitter. Isolate the ADC clock from any digital circuitry with buffers, as with the clock tree shown in *Figure 6*. The gates used in the clock tree must be capable of operating at frequencies much higher than those used if added jitter is to be prevented.

Best performance will be obtained with a differential input drive, compared with a single-ended drive, as discussed in Sections 2.2.1 and 2.2.2.

As mentioned in Section 3.1, it is good practice to keep the ADC clock line as short as possible and to keep it well away from any other signals. Other signals can introduce jitter into the clock signal, which can lead to reduced SNR performance, and the clock can introduce noise into other lines. Even lines with 90° crossings have capacitive coupling, so try to avoid even these 90° crossings of the clock line.

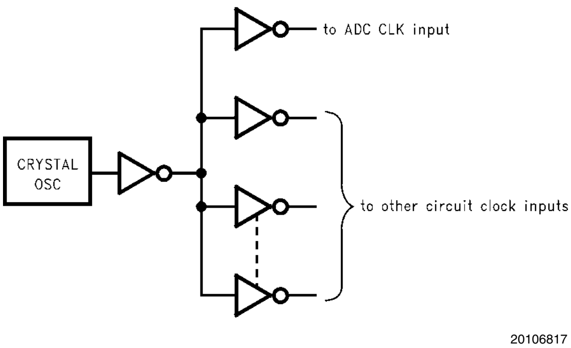


FIGURE 6. Isolating the ADC Clock from other Circuitry with a Clock Tree

8.0 COMMON APPLICATION PITFALLS

Driving the inputs (analog or digital) beyond the power supply rails. For proper operation, all inputs should not go more than 100 mV beyond the supply rails (more than 100 mV below the ground pins or 100 mV above the supply pins). Exceeding these limits on even a transient basis may cause faulty or erratic operation. It is not uncommon for high speed digital components (e.g., 74F and 74AC devices) to exhibit overshoot or undershoot that goes above the power supply or below ground. A resistor of about 47Ω to 100Ω in series with any offending digital input, close to the signal source, will eliminate the problem.

Do not allow input voltages to exceed the supply voltage, even on a transient basis. Not even during power up or power down.

Be careful not to overdrive the inputs of the ADC12QS065 with a device that is powered from supplies outside the range of the ADC12QS065 supply. Such practice may lead to conversion inaccuracies and even to device damage.

Using an inadequate amplifier to drive the analog input. As explained in Section 1.3, the capacitance seen at the input alternates between two values depending upon the phase of the clock. This dynamic load is more difficult to drive than is a fixed capacitance.

If the amplifier exhibits overshoot, ringing, or any evidence of instability, even at a very low level, it will degrade performance. A small series resistor at each amplifier output and a capacitor at the analog inputs (as shown in *Figure 4* and *Figure 5*) will improve performance. The LMH6550 is an example of an amplifier that may be used to drive the analog inputs of the ADC12QS065.

Also, it is important that the signals at the two inputs have exactly the same amplitude and be exactly 180º out of phase with each other. Board layout, especially equality of the length of the two traces to the input pins, will affect the effective phase between these two signals. Remember that an operational amplifier operated in the non-inverting configuration will exhibit more time delay than will the same device operating in the inverting configuration.

Operating with the reference pins outside of the specified range. As mentioned in Section 1.2, V_{REF} should be in the range of

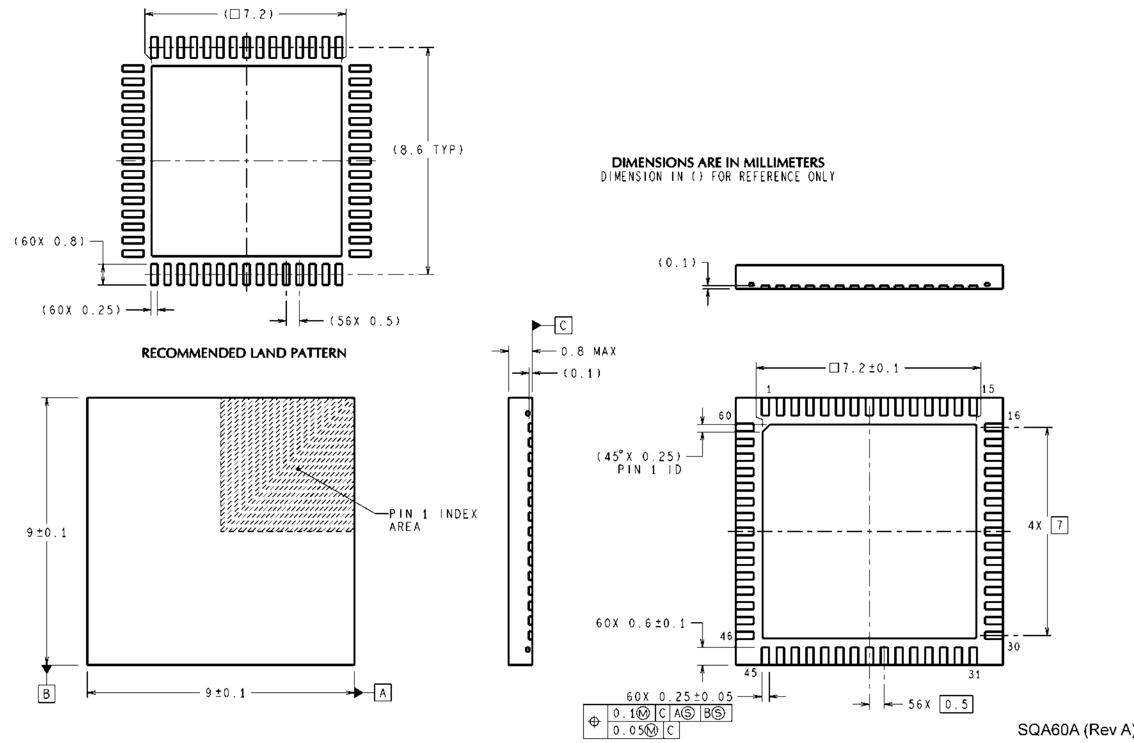
$$0.8V \le V_{REF} \le 1V$$

Operating outside of these limits could lead to performance degradation.

Inadequate network on Reference Bypass pins (VREFT12, VREFB12, VCOM12, VREFT34, VREFB34 and VCOM34). These pins should be bypassed as mentioned in Section 2.1 for best performance.

Using a clock source with excessive jitter, using excessively long clock signal trace, or having other signals coupled to the clock signal trace. This will cause the sampling interval to vary, causing excessive output noise and a reduction in SNR and SINAD performance.

Physical Dimensions inches (millimeters) unless otherwise noted



60-Lead LLP Package
Ordering Number ADC12QS065CISQ
NS Package Number SQA60A

Notes

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